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CLEAN VERSION OF PENDING CLAIMS

HORIZONTAL MEMORY DEVICES WITH VERTICAL GATES
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Claims 1-23, as of August 29, 2002, date response was filed.

1. (Amended) A memory cell, comprising:

a source region in a horizontal substrate;

a drain region in the horizontal substrate;

a channel region separating the source and the drain regions;

an edge-defined vertical floating gate located above a portion of the channel region and separated from the channel region by a first thickness insulator material;

at least one edge-defined vertical control gate located above another portion of the channel region and separated therefrom by a second thickness insulator material, wherein the at least one vertical control gate is parallel to and opposing the vertical floating gate, and wherein the at least one vertical control gate is separated from the vertical floating gate by an intergate dielectric; and

wherein a floating gate capacitance associated with the edge-defined floating gate is smaller than a control gate capacitance associated with the at least one edge-defined vertical control gate.

2. The memory cell of claim 1, wherein the at least one vertical control gate has a horizontal width of approximately 100 nanometers (nm).

3. The memory cell of claim 1, wherein the first thickness insulator material is approximately 60 Angstroms (Å), and wherein the second thickness insulator material is approximately 100 Angstroms (Å).

4. The memory cell of claim 1, wherein the first thickness insulator material, the second thickness insulator material, and the intergate dielectric include silicon dioxide (SiO_2).

5. The memory cell of claim 1, wherein the vertical floating gate has a vertical height of approximately 500 nanometers (nm) and a horizontal width of approximately 100 Angstroms (Å).

6. The memory cell of claim 1, wherein the intergate dielectric has a thickness approximately equal to the first thickness insulator material.

7. (Amended) A transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

an edge-defined vertical floating gate separated from a first portion of the channel region by a first oxide thickness;

at least one edge-defined vertical control gate separated from a second portion of the channel region by a second oxide thickness, wherein the at least one vertical control gate is parallel to and opposing the vertical floating gate; and

wherein a floating gate capacitance associated with the edge-defined floating gate is smaller than a control gate capacitance associated with the at least one edge-defined vertical control gate.

8. The transistor of claim 7, wherein the vertical floating gate has a vertical height of approximately 500 nanometers (nm) and a horizontal width of approximately 100 nanometers (nm).

9. The transistor of claim 7, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).

10. The transistor of claim 7, wherein the at least one vertical control gate has a horizontal width of approximately 100 Angstroms (Å).

11. The transistor of claim 7, wherein the vertical floating gate separated from a first portion of the channel region includes a first portion of the channel region which is adjacent to the source region, and wherein the at least one vertical control gate separated from a second portion of the channel region includes a second portion of the channel region which is adjacent to the drain region.

12. The transistor of claim 11, wherein the at least one vertical control gate further includes a horizontal member located above the vertical floating gate, wherein the at least one vertical control gate an the horizontal member are separated from the vertical floating gate by an intergate dielectric.

13. The transistor of claim 7, wherein a capacitance between the at least one vertical control gate and the floating gate is greater than a capacitance between the floating gate and the channel.

14. (Amended) A floating gate transistor, comprising:

a horizontal substrate, wherein the substrate includes a source region, a drain region, and a channel region separating the source and the drain region;

a first edge-defined vertical gate located above a first portion of the channel region and separated from the channel region by a first oxide thickness;

a second edge-defined vertical gate located above a second portion of the channel region and separated from the channel region by a second oxide thickness;

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a third edge-defined vertical gate located above a third portion of the channel region and separated from the channel region by the second oxide thickness; and

wherein a first capacitance associated with one of the vertical gates is smaller than a second capacitance associated with the remaining vertical gates.

15. The floating gate transistor of claim 14, wherein the second and the third vertical gates are parallel to and on opposing sides of the first vertical gate.

16. The floating gate transistor of claim 14, wherein the first vertical gate includes a floating gate and wherein the second and the third vertical gates include control gates.

17. The floating gate transistor of claim 14, wherein first vertical gate includes a control gate and wherein the second and the third vertical gates include floating gates.

18. The floating gate transistor of claim 14, wherein the floating gate transistor further includes a horizontal gate member which couples the second and the third vertical gates.

19. The floating gate transistor of claim 14, wherein a greater percentage of a voltage applied to the second and the third vertical gates appears between the first vertical gate and the channel than between the first vertical gate and the second and the third vertical gates.

20. The floating gate transistor of claim 14, wherein the second and the third portion of the channel region are adjacent the source region and the drain region, respectively.

21. The floating gate transistor of claim 14, wherein the first vertical gate, the second vertical gate, and the third vertical gate include polysilicon gates which are separated from one another by silicon dioxide (SiO_2).

22. The floating gate transistor of claim 14, wherein the first vertical gate, the second vertical gate, and the third vertical gate each have a horizontal width of approximately 100 nanometers (nm).

23. The floating gate transistor of claim 14, wherein the first oxide thickness is approximately 60 Angstroms (Å), and wherein the second oxide thickness is approximately 100 Angstroms (Å).